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Claims

[c1] What is claimed is:

1.An integrated circuit chip test apparatus comprising:

a module test fixture having contact pads, wherein said contact pads are adapted to make contact with signal input/output pins on an integrated circuit chip being tested;

an intermediate banking box connected to said module text fixture; and

a tester connected to said intermediate banking box, wherein said tester includes at least one bank of channels, wherein there are more of said pins on said integrated circuit chip than there are said channels in said tester,

wherein said intermediate banking box includes switches connected between said contact pads and said channels, and

wherein said switches are adapted to selectively connect a subset of said contact pads to said channels to connect said tester to a subset of said pins, thereby allowing said tester to test a portion of said integrated circuit that corresponds to said subset of pins.

[c2] 2.The apparatus in claim 1, wherein selected dedicated channels of said channels are dedicated to specific ones of said pins and are not switched to different pins during chip testing.

[c3] 3.The apparatus in claim 2, wherein said dedicated channels comprise flex channels that can change which pin connections said dedicated channels are dedicated to when testing different types of chips.

[c4] 4.The apparatus in claim 1, wherein said intermediate banking box comprises a plurality of banks of said channels and further comprises a multiplexor controller for coordinating the connections of said banks.

[c5] 5.The apparatus in claim 4, wherein said banks are connected in parallel within said banking box.

[c6] 6.The apparatus in claim 1, wherein a full chip test program supplied to said tester is modified by said tester such that said tester sequentially applies portions of said full chip test program to portions of said integrated circuit as limited by the number of channels.

[c7] 7.The apparatus in claim 1, wherein said intermediate banking box is adapted to be connected to a plurality of different module text fixtures associated with different types of integrated chips to be tested, such that said in-

termediate banking box can be used to test a plurality of different pin style integrated circuit chips.

[c8] 8.An integrated circuit chip test apparatus comprising:
a module test fixture having contact pads, wherein said contact pads are adapted to make contact with signal input/output pins on an integrated circuit chip being tested;
a tester connected to said module test fixture,
wherein said tester includes at least one bank of channels, wherein there are more of said pins on said integrated circuit chip than there are said channels in said tester,
wherein said tester also includes switches connected between said contact pads and said channels, and
wherein said switches are adapted to selectively connect a subset of said contact pads to said channels to connect said tester to a subset of said pins, thereby allowing said tester to test a portion of said integrated circuit that corresponds to said subset of pins.

[c9] 9.The apparatus in claim 8, wherein selected dedicated channels of said channels are dedicated to specific ones of said pins and are not switched to different pins during chip testing.

[c10] 10.The apparatus in claim 2, wherein said dedicated

channels comprise flex channels that can change which pin connections said dedicated channels are dedicated to when testing different types of chips.

[c11] 11.The apparatus in claim 8, wherein said switches comprise a plurality of banks of said channels and further comprise a multiplexor controller for coordinating the connections of said banks.

[c12] 12.The apparatus in claim 11, wherein said banks are connected in parallel.

[c13] 13.The apparatus in claim 8, wherein a full chip test program supplied to said tester is modified by said tester such that said tester sequentially applies portions of said full chip test program to portions of said integrated circuit as limited by the number of channels.

[c14] 14.The apparatus in claim 8, wherein said tester is adapted to be connected to a plurality of different module text fixtures associated with different types of integrated chips to be tested, such that said intermediate banking box can be used to test a plurality of different pin style integrated circuit chips.

[c15] 15.An integrated circuit chip test apparatus comprising: a module test fixture having contact pads, wherein said contact pads are adapted to make contact with signal in-

put/output pins on an integrated circuit chip being tested;

an intermediate banking box connected to said module text fixture; and

a tester connected to said intermediate banking box, wherein said tester includes at least one bank of channels, wherein there are more of said pins on said integrated circuit chip than there are said channels in said tester,

wherein said intermediate banking box includes switches connected between said contact pads and said channels, wherein said switches are adapted to selectively connect a subset of said contact pads to said channels to connect said tester to a subset of said pins, thereby allowing said tester to test a portion of said integrated circuit that corresponds to said subset of pins, and

wherein said intermediate banking box is adapted to be used with a plurality of different module test fixtures and testers.

[c16] 16.The apparatus in claim 15, wherein selected dedicated channels of said channels are dedicated to specific ones of said pins and are not switched to different pins during chip testing.

[c17] 17.The apparatus in claim 16, wherein said dedicated channels comprise flex channels that can change which

pin connections said dedicated channels are dedicated to when testing different types of chips.

[c18] 18.The apparatus in claim 15, wherein said intermediate banking box comprises a plurality of banks of said channels and further comprises a multiplexor controller for coordinating the connections of said banks.

[c19] 19.The apparatus in claim 18, wherein said banks are connected in parallel within said banking box.

[c20] 20.The apparatus in claim 15, wherein a full chip test program supplied to said tester is modified by said tester such that said tester sequentially applies portions of said full chip test program to portions of said integrated circuit as limited by the number of channels.